Circuit Design for ESD and Supply Noise Mitigation

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ABSTRACT
One of the (anonymous peer) reviewers of a recent paper from our group wrote that power-on ESD (e.g., powered IEC 61000-4-2) is a “hot topic” and evaluating chips under those conditions is becoming “increasingly common,” especially for automotive applications. That hot topic is the subject of this presentation.

Of particular concern is the case that a portion of the ESD current enters a chip IO pin. The presentation will begin with an examination of the paths by which ESD noise is transmitted from the IO supply to the other supplies on-chip. The noise amplitude is affected by the design of the ground distribution network and the integrated voltage regulators.

Latch-up is another consequence of power-on ESD. Reverse body bias is a technique used to place circuitry in a low-power (e.g., sleep) mode. For the NMOS transistors, there are two general approaches to generating the body bias: pump the P-wells to a lower potential than VSS, or ground the P-substrate and regulate the VSS bus voltage. We have identified that the latter approach may cause latch-up to occur during power-on ESD. The latch-up threshold is affected by the placement of the regulator’s pass transistor, the ESD protection network implementation, and the VSS net resistance.

Chips that are intended to survive some level of power-on ESD stress cannot utilize ESD protection circuitry that is inactivated when the power is on. Rail clamp circuits that provide protection against power-on ESD may also reduce the amplitude of supply noise due to simultaneous switching noise. The benefit gained depends on the frequency spectrum of the noise. Circuit simulation shows clearly the noise improvement from a well-designed rail clamp circuit but measuring the chip-level supply noise has proved to be challenging due to noise generated at the board-level. Time permitting, I will share details of the multiple board designs we have tested and solicit the attendees’ suggestions for our next re-spin.